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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,082	10/30/2003	Armin Willmeroth	MUH-12838	9900

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EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,082	WILLMEROTH ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-20* is/are pending in the application.

4a) Of the above claim(s) *5-12 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 14-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claims 5-12 and 20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on November 1, 2004.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, and 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kusunoki (US Pat. 6,323,509) in view of Tanaka (US PgPub 2001/0040255, hereinafter Tanaka).

Regarding claims 1 and 19, Figure 1 of Kusunoki discloses an IGBT with a monolithically integrated antiparallel diode, comprising: a semiconductor substrate 1 forming an inner zone and having a front side, a rear side, and a peripheral high-voltage edge (region where p-regions 28 are located); said front side of said semiconductor substrate having semiconductor wells 8 of a first conductivity type (p-type) formed therein with transistor cells within said peripheral high-voltage edge; at least one emitter region 4 of the first conductivity type formed at said rear side of said semiconductor substrate; at least one emitter short region 6 of a second conductivity type (n-type) integrated substantially only in a region of said high voltage edge, said

at least one emitter short region lying in a plane with said at least one emitter region and forming an electrode of the antiparallel diode; said at least one emitter region having no emitter short regions within said high-voltage edge; and said semiconductor wells on said front side of said semiconductor substrate forming a counterelectrode of the antiparallel diode. Note that it is considered that the gate electrodes 11 dissect region 8 into a plurality of separate wells. Also note that the limitation "doping with a dose of between 1 x 10^{12} and 1 x 10^{15} charge carriers per cm^2" is merely a product-by-process limitation. The specified dose (which is a process step) does not necessarily impart a specific dopant concentration. Therefore, the product-by-process limitation does not structurally/patentably the claimed product over the prior art. Since the structure shown in Figure 1 of Kusunoki does not physically change, the distance between a point located at the center of the IGBT and said emitter short region is maximized for triggering the IGBT at the lowest possible current. In other words, for the particular device shown in Figure 1, whatever current causes the IGBT to trigger is the lowest possible current, and therefore the distance can be considered maximized. The difference between Kusunoki and the claimed invention is the emitter region having a thickness less than 1 micrometer. Figures 10 and 11 of Tanaka disclose an IGBT comprising an emitter region 2B having a thickness of 0.8 microns (paragraph [0187]). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kusunoki by using the emitter thickness of Tanaka for the purpose of increasing the turn-off speed of the IGBT (paragraph [0190] of Tanaka). Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Kusunoki by using the claimed thickness value, since it has been held that where the general conditions of

a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Assuming, *arguendo*, that the limitation "doping with a dose of between 1 x 10^{12} and 1 x 10^{15} charge carriers per cm^{2}" does structurally distinguish the claimed invention over Kusunoki, it would have still been obvious to use a dose within the claimed range as taught by Tanaka (1x10^{13}ions/cm^{2}) (paragraph [0198]) for the purpose of obtaining the above mentioned thickness (paragraph [0198]).

Regarding claim 2, Figure 1 of Kusunoki discloses said semiconductor wells 8 at least predominately contain transistor cells.

Regarding claim 14, Kusunoki discloses a lifetime of minority charge carriers in said semiconductor substrate 1 is at least 10 microseconds (col. 19, lines 49-51 and col. 20, lines 5 and 6).

Regarding claim 15, a further difference between Kusunoki and the claimed invention is a thickness of said inner zone formed by said substrate is less than 200 μm. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Kusunoki by using the claimed thickness, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 16, Figure 1 of Kusunoki discloses a field stop region (buffer region) 3 of the second conductivity type (n-type) integrated between a first region including said substrate 1 and a second region including said emitter region 4 and emitter short region 6.

Regarding claim 17, Kusunoki discloses the impurity concentration of the substrate is 1 x 10^{13}-1 x 10^{15} /cm^3 (col. 16, lines 12-15) and the impurity concentration of the emitter region is 1 x 10^{17}-1 x 10^{21} /cm^3. Therefore, the emitter region is doped significantly higher than the emitter.

Regarding claim 18, the product-by-process limitation "wherein said at least one emitter region is annealed at a temperature of less than 600°C" does not structurally/patentably distinguish the claimed invention over the prior art.

Claims 1-4 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa et al. (US Pat. 4,689,647, hereinafter Nakagawa) in view of Tanaka.

Regarding claims 1 and 19, Figure 6 of Nakagawa discloses an IGBT with a monolithically integrated antiparallel diode, comprising: a semiconductor substrate 12 forming an inner zone and having a front side, a rear side, and a peripheral high-voltage edge (region to the right of region 14-4); said front side of said semiconductor substrate having semiconductor wells (13-1 and 13-2) of a first conductivity type (p-type) formed therein with transistor cells within said peripheral high-voltage edge; at least one emitter region 11 of the first conductivity type formed at said rear side of said semiconductor substrate; at least one emitter short region 21 of a second conductivity type (n-type) integrated substantially only in a region of said high voltage edge, said at least one emitter short region lying in a plane with said at least one emitter region and forming an electrode of the antiparallel diode; said at least one emitter region having no emitter short regions within said high-voltage edge; and said semiconductor wells on said front side of said semiconductor substrate forming a counterelectrode of the antiparallel diode. Note that the limitation "doping with a dose of between 1 x 10^{12} and 1 x 10^{15} charge carriers per

cm^2" is merely a product-by-process limitation. The specified dose (which is a process step) does not necessarily impart a specific dopant concentration. Therefore, the product-by-process limitation does not structurally/patentably the claimed product over the prior art. Since the structure shown in Figure 6 of Nakagawa does not physically change, the distance between a point located at the center of the IGBT and said emitter short region is maximized for triggering the IGBT at the lowest possible current. In other words, for the particular device shown in Figure 6, whatever current causes the IGBT to trigger is the lowest possible current, and therefore the distance can be considered maximized. The difference between Nakagawa and the claimed invention is the emitter region having a thickness less than 1 micrometer. Figures 10 and 11 of Tanaka disclose an IGBT comprising an emitter region 2B having a thickness of 0.8 microns (paragraph [0187]). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Nakagawa by using the emitter thickness of Tanaka for the purpose of increasing the turn-off speed of the IGBT (paragraph [0190] of Tanaka). Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Nakagawa by using the claimed thickness value, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Assuming, *arguendo*, that the limitation "doping with a dose of between 1×10^{12} and 1×10^{15} charge carriers per cm^2" does structurally distinguish the claimed invention over Nakagawa, it would have still been obvious to use a dose within the claimed range as taught by Tanaka ($1x10^{13}$ions/cm^2) (paragraph [0198]) for the purpose of obtaining the above mentioned thickness (paragraph [0198]).

Regarding claim 2, Figure 6 of Nakagawa discloses said semiconductor wells (13-1 and 13-2) at least predominately contain transistor cells.

Regarding claim 3, Figure 6 of Nakagawa discloses said at least one emitter short region 21 reaches as far as a chip end in edge portions of the IGBT.

Regarding claim 4, Figure 6 of Nakagawa discloses edge regions of the IGBT contain an emitter region 11 at said high-voltage edge.

Regarding claim 15, Figure 6 of Nakagawa discloses a thickness of said inner zone formed by said substrate 12 is less than 200μm (col. 3, lines 43-45).

Regarding claim 16, Figure 6 of Nakagawa discloses a field stop region 10 of the second conductivity type (n-type) integrated between a first region including said substrate 12 and a second region including said emitter region 11 and emitter short region 21.

Regarding claim 17, Nakagawa discloses the emitter region 11 is doped significantly higher than substrate 12 (col. 3, lines 41-44).

Regarding claim 18, the product-by-process limitation "wherein said at least one emitter region is annealed at a temperature of less than 600°C" does not structurally/patentably distinguish the claimed invention over the prior art.

Response to Arguments

Applicant's arguments filed September 21, 2005 have been fully considered but they are not persuasive.

Applicant argues that neither Kusunoki nor Nakagawa disclose "a distance between a point located at the center of the IGBT and the emitter short region being maximized for triggering the IGBT at a lowest possible current". However, the above limitation does not require any particular distance. As explained in the above rejection, since the devices of Kusunoki and Nakagawa are finished products that do not physically change, the distance between a point located at the center of the IGBT and the emitter short region does not change. Therefore, regardless of the value for that distance, it can be considered "maximized" for that particular device. In other words, there is only one value for that distance, and that one value can be considered the maximum value. It follows that whatever current triggers the IGBT is the lowest possible current for that particular device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew C. Landau

October 30, 2005